ABSTRACT

A pipelined, simultaneous and redundantly threaded ("SRT") processor configured to detect transient faults during program execution by executing instructions in at least two redundant copies of a program thread. The processor comprises load/store units configured to perform fetch and store operations to or from data sources and a load value queue for storing the data values fetched in response to data fetch instructions in a first program thread. The load/store units place a duplicate copy of the data in the load value queue after fetching the data from the data source and retiring the load instruction in the first thread. The load/store units access the load value queue and not the data source to fetch data values in response to corresponding data fetch instructions in the second program thread.